greater performance levels. Our initial major assumption is that applying E-Hard (evolvable hardware) techniques to the wafer would result in the evolution adapting to the inevitable fabrication faults of the wafer. The wafer's much greater area compared to a chip could then contain one huge circuit, consisting of all four components of E-Hard, i.e., the chromosomes used to evolve the circuit, the circuit itself, the hardware-compiled fitness definition, and the GA management. Wafer-scale E-Hard would be the ultimate in speed. The next assumption concerned the diameter of the wafer. A state-of-the-art wafer is 12 inches, at 2.5cm per inch, and considering that a Xilinx XC6264 chip has a surface area of roughly a square centimeter, that means that the wafer should be roughly 750 times greater in area. The CBM consists of about 50 chips of 1cm² each, so the wafer should be about 15 times greater in area than the CBM. Implementing a wafer would imply using ASIC (application-specific integrated circuit) techniques, which are about four times denser than FPGAs. Clocking at about 30 MHz and with 9000 CoDi cells in the CBM implies about 15 4 9000 CoDi cells in the wafer, i.e., 500,000. (Of course this is an upper bound, because space would be needed for the other three E-Hard components – the chromosomes, the fitness definition, and the GA control.) The total CA cell update rate of a wafer-CAM would be 500,000 CoDi cells at 30MHz, i.e., 15 trillion/s, or some 150 times faster than the CBM. The greater area and speed would probably allow the chromosomes to be grown and their fitness measured in parallel. If building this wafer is not too expensive, we would like to investigate the possibility of applying the CoDi model to WSI, particularly now that that WSI is commercial. (There are now WSI companies in Silicon Valley.)

References
(Note: Any paper containing the name de Garis, can be downloaded from his web site at URL: http://www.shipa.stanford.edu/~degaris)